

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY GURAJADA VIZIANAGARAM
III B. Tech I Semester Regular/Supplementary Examinations, April/May -2025
LINEAR IC APPLICATIONS

(ELECTRICAL AND ELECTRONICS ENGINEERING)

Time: 3 hours

Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**

All Questions Carry Equal Marks

		UNIT-I	
1.	a)	Explain the concept of Common Mode Rejection Ratio (CMRR) in an Op-Amp and describe a method to measure it.	[7M]
	b)	Define input bias current and input offset current for an Op-Amp and discuss their effects on circuit performance.	[7M]
		(OR)	
2.	a)	An Op-Amp has a slew rate of $1.5 \text{ V}/\mu\text{s}$. What is the maximum frequency of a sinusoidal output voltage with a peak value of 10V before slew rate distortion occurs?	[7M]
	b)	Draw and explain the differential amplifier stage of an Op-Amp.	[7M]
		UNIT-II	
3.	a)	Derive the expression for the gain of an inverting Op-Amp amplifier.	[7M]
	b)	With a neat sketch, explain the operation of a precision rectifier and discuss its advantages over a regular diode rectifier.	[7M]
		(OR)	
4.	a)	Design an Op-Amp circuit to perform the mathematical operation of subtraction of two input signals. Derive the expression for the output.	[7M]
	b)	Discuss the operation of an Op-Amp as a differentiator.	[7M]
		UNIT-III	
5.	a)	Explain the operation of a wide band-pass filter and provide a design procedure. Include a suitable circuit diagram.	[7M]
	b)	Design a second-order high-pass filter with a cutoff frequency of 2 kHz using an Op-Amp.	[7M]
		(OR)	
6.	a)	Design a second-order Butterworth high-pass filter with a cutoff frequency of 1.5 kHz. Assume a suitable damping factor.	[7M]
	b)	Describe the operation of a peak detector circuit with a suitable diagram.	[7M]
		UNIT-IV	
7.	a)	Draw the circuit diagram of a 555 timer connected as an astable multivibrator. Explain how the duty cycle of the output waveform can be adjusted.	[7M]
	b)	Explain the principle of operation of a Phase-Locked Loop (PLL).	[7M]
		(OR)	
8.	a)	Explain the operation of a monostable multivibrator using a 555 timer. Derive the expression for the pulse width of the output.	[7M]
	b)	Draw a block diagram illustrating how a PLL can be used for FM demodulation. Explain the demodulation process.	[7M]
		UNIT-V	
9.	a)	Draw the circuit of an Inverted R-2R ladder DAC and derive the expression for the output voltage.	[7M]
	b)	Discuss the working principle of a flash ADC.	[7M]
		(OR)	
10.	a)	Explain the operation of a switched capacitor DAC with neat diagrams.	[7M]
	b)	With a clear block diagram, explain the operation of a sigma-delta ADC.	[7M]
